REMARKS

Claims 1-22 remain pending in the instant application. All claims presently stand rejected. Claim 1 is presently amended. Applicants respectfully request reconsideration of the application and allowance of all the pending claims in view of the above amendments and the following remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of US Patent No. 5,862,314 to Jeddeloh ("*Jeddeloh*"), US Patent No. 6,189,111 B1 to Alexander et al. ("*Alexander*"), US Application Serial No. 2003/0154392A1 to Lewis ("*Lewis*"), US Patent No. 5,592,616 to Finch et al. ("*Finch*"), US Application Serial No. 2003/0177129A1 to Bond et al. ("*Bond*") and Wikipedia ("*Wikipedia*").

Specifically, claims 1-4, 8-12 and 16-18 are rejected as being unpatentable over *Jeddeloh* in view of *Alexander*, claims 5, 6, 14 and 20 are rejected as being unpatentable over *Jeddeloh* in view of *Alexander* and in further view of *Lewis*, claim 7 is rejected as being unpatentable over *Jeddeloh* in view of *Alexander* in further view of *Finch*, claims 13 and 19 are rejected as being unpatentable over *Jeddeloh* in view of *Alexander* in further view of *Bond* and claims 15 and 21 are rejected as being unpatentable over *Jeddeloh* in view of *Alexander* in view of *Lewis* in further view of *Wikipedia*. Finally, claim 22 is rejected as being unpatentable over *Jeddeloh* in view of *Alexander* in further view of *Wikipedia*.

Applicants respectfully traverse the Examiner's rejections. To establish a *prima facie* case of obviousness, three criteria must be met: (1) the prior art references must teach or suggest all the claim limitations; (2) some suggestion or motivation to combine the references must be found in the prior art; and (3) there must be a reasonable expectation of success. MPEP § 2143. As explained below, Applicants respectfully submit that a *prima facie* case of obviousness has not been established in this case.

Amended claim 1 recites (emphasis added):

detecting a faulty portion of memory in a computer system <u>during an operating system runtime</u>, the faulty portion having stored a system software component in a system software memory region of memory; and

relocating the system software component from the faulty portion of memory to a safe portion of memory.

According to the Examiner, *Jeddeloh* discloses detecting a faulty portion of memory in a computer system, the faulty portion having stored in a system software memory region of memory; and relocating from the faulty portion of memory to a safe portion of memory. The Examiner concedes the *Jeddeloh* does not disclose a system software component and relocating the system software component, but alleges that *Alexander* discloses critical information resources that are equivalent to a system software component. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a system software component and relocate the system

software component because this information is important for the running of the computing system.

Applicants respectfully disagree. Even if the Examiner's characterization of *Alexander's* critical information resources as a "system software component" is correct, which Applicants do not concede, *Jeddeloh* still would not disclose the claimed combination because *Jeddeloh* fails to disclose "detecting a faulty portion of a memory in a computer system <u>during an operating system runtime</u>." *Jeddeloh* is directed to a system and method for remapping defective memory locations. As such, *Jeddeloh* teaches storing an error map 18 that identifies defective memory portions of a memory module. Computer system 10 uses error map 18 to avoid use of defective memory portions. Error map 18 is preferably created in a factory that makes the memory block (col. 3, lines 3-5). Thus, faulty memory portions have been detected and mapped well before an operating system ("OS") runtime. Furthermore, Applicants have reviewed column 4, lines 19-48, as directed by the Examiner with respect to the rejection of independent claim 10, and have not been able to find any reference to access of error map 18 during an OS runtime.

Therefore, *Jeddeloh* fails to disclose or fairly suggest "detecting a faulty portion of memory in a computer system <u>during an operating system runtime,</u>" as expressly claimed by the Applicants. Applicants respectfully submit that *Alexander* also fails to disclose "detecting a faulty portion of memory in a computer system during an operating system runtime," as expressly claimed by

the Applicants. Thus, Jeddeloh and Alexander fail to disclose every element and limitation recited in the claim, and therefore, on that basis alone, cannot obviate the claim.

Not only do *Jeddeloh* and *Alexander* fail to disclose every element and limitation of claim 1, there is no motivation to combine the references because *Jeddeloh* actually **teaches against** the combination as suggested by the Examiner. Amended claim 1 recites, in pertinent part, "**detecting** a faulty portion of memory in a computer system ...the faulty portion having stored a system software component" AND "**relocating** the system software component from the faulty portion of memory to a safe portion of memory."

As discussed above, *Jeddeloh* is directed to a system and method for remapping defective memory locations. *Alexander* is directed to resource harvesting in scalable, fault tolerant, single system image clusters. *Jeddeloh* teaches storing an error map 18 that identifies defective memory portions of a memory module. Thus, the error map is used so that the processor does not access and write to defective memory portions. As such, relocation of system software components are not an issue, since in *Jeddeloh*, the purpose is to **prevent** a component from being written to a defective memory portion in the first place. Thus, Jeddeloh actually **teaches against** the "relocating [[of]] the system software component" because its purpose is to eliminate the need to relocate components stored in defective memory portions. Accordingly, there is

no motivation to combine *Jeddeloh* with *Alexander*, as required under M.P.E.P. § 2143 to establish a prima facie case of obviousness.

Consequently, the combination of *Jeddeloh* and *Alexander* fail to teach or suggest all elements of claim 1, as required under M.P.E.P. § 2143.03. Independent claims 10 and 17 include similar nonobvious elements as independent claim 1. Accordingly, Applicants request that the instant §103(a) rejections of claims 1, 10 and 17 be withdrawn.

The dependent claims are nonobvious over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 103(a) rejections of the dependent claims be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.
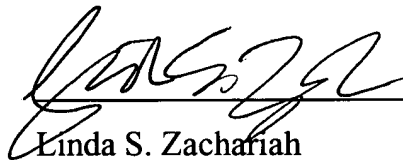
CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 11·21·06

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